

A simple but complicated mosfet amplifier



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Schematics

Below is the schematic of a single amplifier channel, which includes a linear power supply. The input voltage is 30V, provided by a Connex Electronics SMPS300RS. The regulator's output voltage is set to 28.5V.

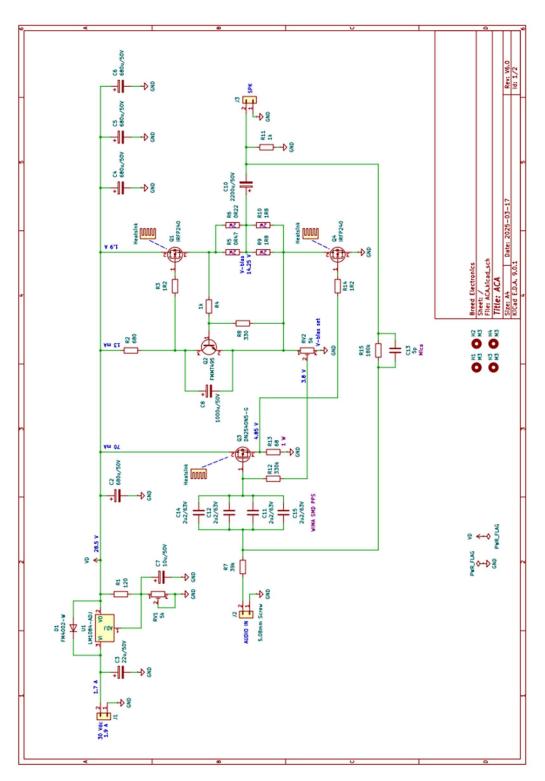


Figure 1 - The amplifier schematics'- page 1

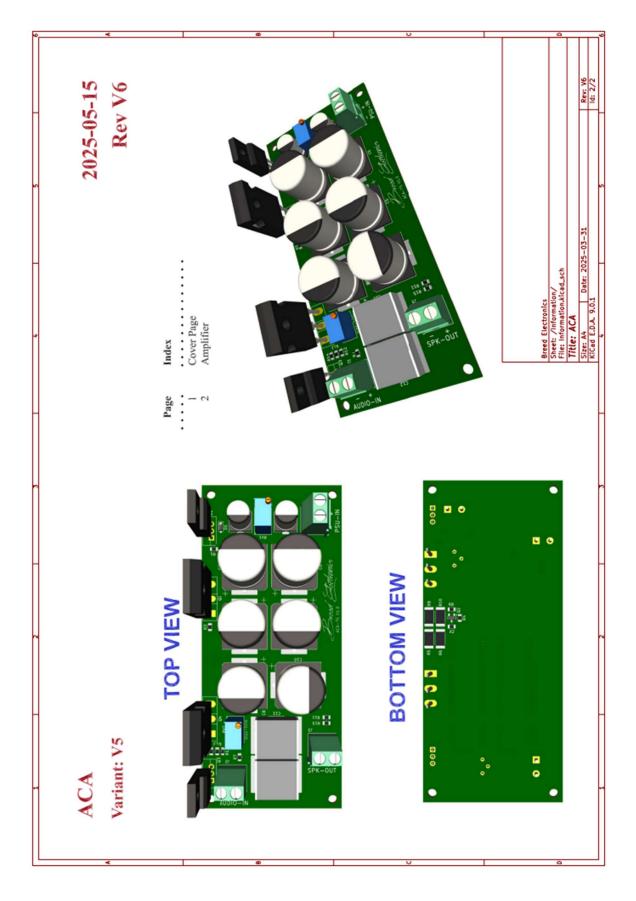
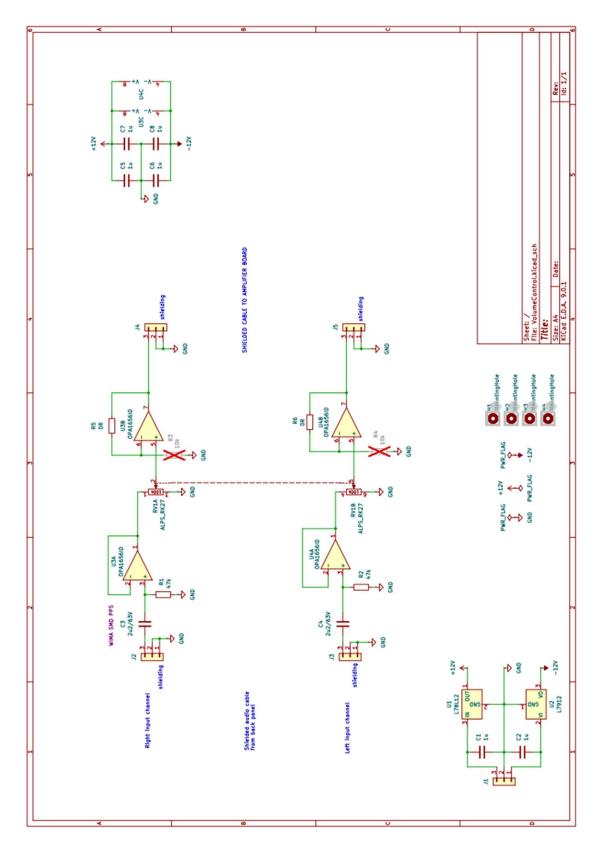


Figure 2 - Amplfier schematics - page 2



Below the schematic of the volume control. The potentiometers are buffered with OPA1656 audio opamps.

Figure 3 - Volume control schematics

PCB Layout

Amplifier pcb has 4 layers. The middle layers are GND and Vd. SMD components are used where possible. The input capacitors are PPS types made by Wima.

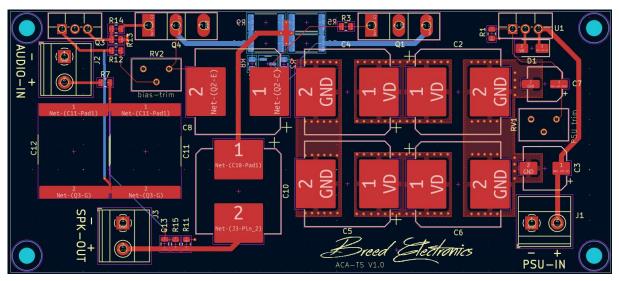


Figure 4 – Amplifier 4-layer pcb design

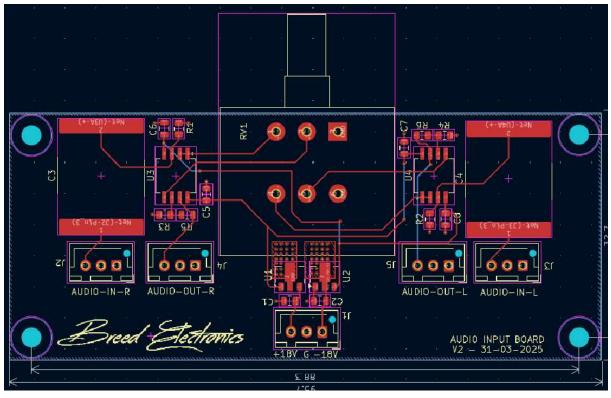


Figure 5 - Volume control 2-layer pcb design

Renders

Renders of amplifier pcb



Figure 6 - Top view



Figure 7 - Back view of amplifier pcb

The bottom side also contains some components

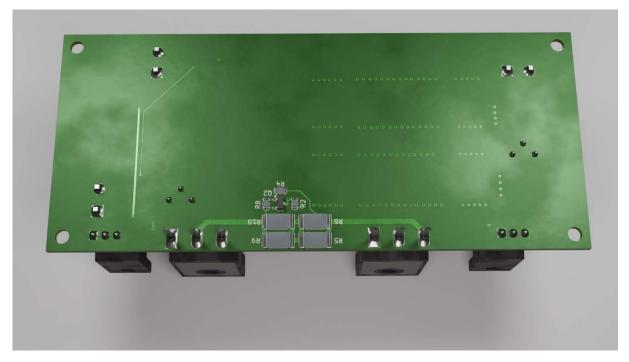


Figure 8 - Bottom view of amplifier pcb

Render of the 2-layer volume control pcb

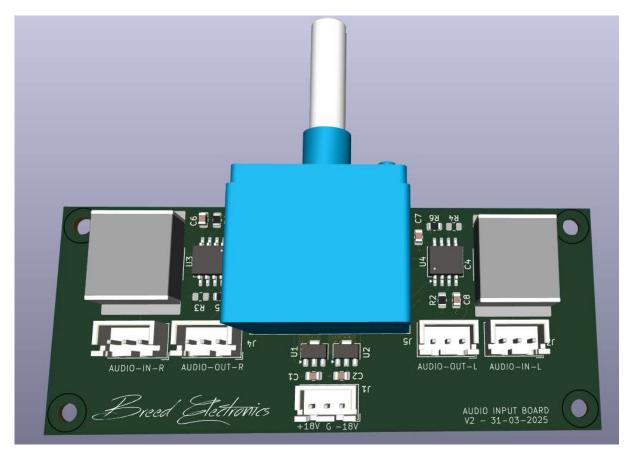


Figure 9 - Top view of volume control pcb

Photos

Photo of actual amplifier

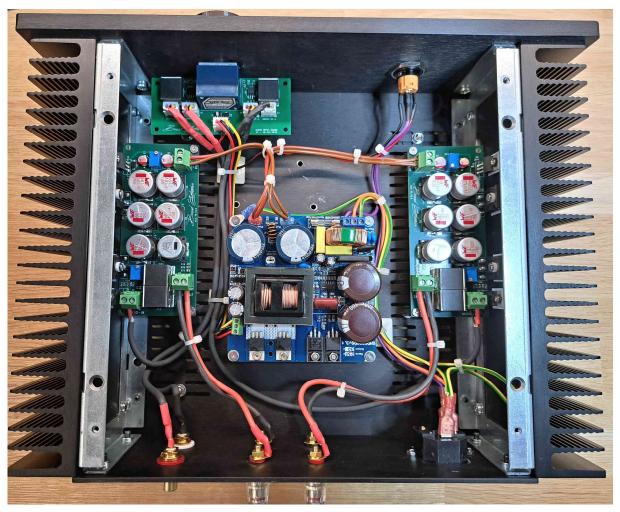


Figure 10 - Amplifier seen from the top



Figure 11 - Amplifier seen from the front

LTspice simulations

Before the amplifier was build simulations where done. All simulations where made with LTspice. Below the schematics as used in LTspice.

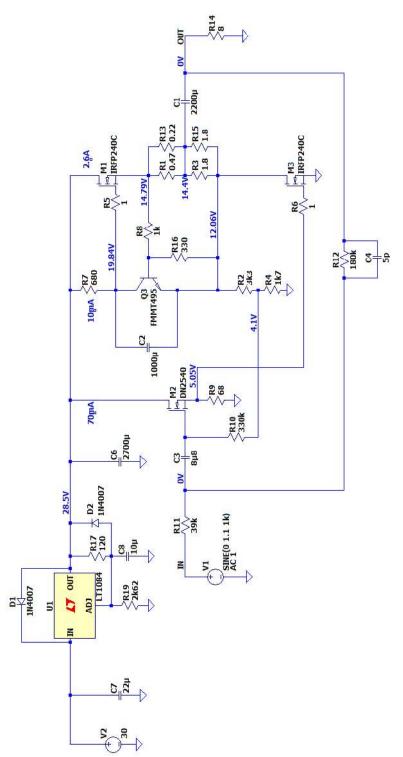


Figure 12 - LTspice schematics

Gain

The gain of the amplifier should be 4.07 / 1.1 = 3.7 = 11.4 dB when simulated (upper image). In practice, it was measured to be 11.6 dB (lower image)

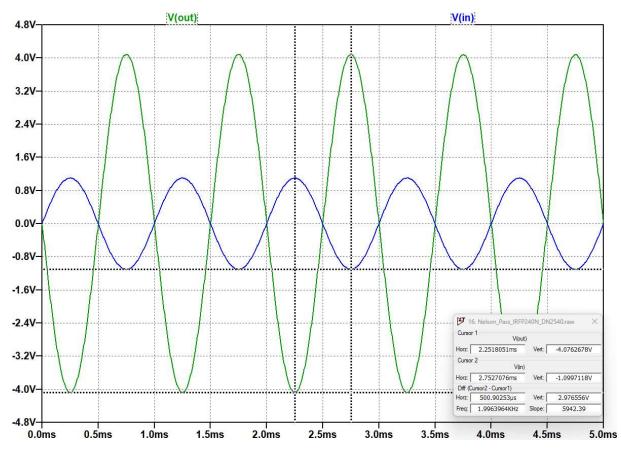


Figure 13 - Simulated input- and output signal

Gain (dB) 14 13 12 11 B3: 89.996 kHz 10 9 8 7 6 5 90.00 4 1 10 20 50 100 200 500 1k 2k 5k 10k 20k 50k 100k 5

Figure 14 - Measured gain vs frequency

Note that the bandwidth shown in the Gain plot is limited by the measurement device (QA403). The actual bandwidth is greater as we will see later.

According to the simulation the THD is 0.008 % at 1 kHz / 1W / 8 Ohm. In practice it was measured to be 0.02 % for the same conditions.

pout: AVG(V(OUT)*I(R14))=1.04071934827 FROM 0 TO 0.005 Fourier components of V(OUT) N-Period=1 DC component:0.00392279 Normalized Phase Normalized Harmonic Frequency Fourier Component 4.081e+00 Phase [deg] Component 1.000e+00 Number [Hz] [degree] -89.79° 1.000e+03 0.00° 1 39.58° 129.37° 2.000e+03 2.358e-04 5.778e-05 2 3.000e+03 2.728e-05 6.685e-06 -134.02° -44.23° 3 4.000e+03 2.197e-05 5.384e-06 88.85° 178.64° 4 5 5.000e+03 2.056e-05 5.038e-06 86.46° 176.25° 89.29° 6 6.000e+03 1.729e-05 4.237e-06 179.09° 89.51° 7 7.000e+03 1.469e-05 3.601e-06 179.30° 89.38° 89.36° 8 8.000e+03 1.286e-05 3.152e-06 179.17° 9 9.000e+03 1.145e-05 2.805e-06 179.15° Partial Harmonic Distortion: 0.005904% Total Harmonic Distortion: 0.007944%

Spectrum analysis

Below a simulated (green) and measured (blue) spectrum of the final amplifier with a 1 kHz signal at +9 dBV (1 W / 8 Ohm). Both show the noise floor so the scale is different.

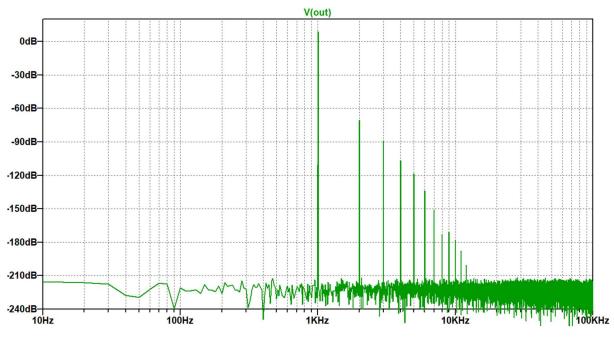


Figure 15 - Simulated spectrum

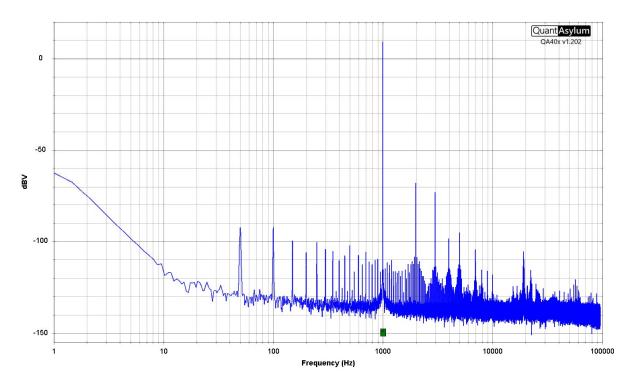


Figure 16 - Measured spectrum

Noise floor

The noise floor at the output of the amplifier when no signal presented at the input is below -90 dBV. Most of the noise is power supply noise. The linear regulator LM1084, the use of SMT components and a 4-layer pcb works quite well.

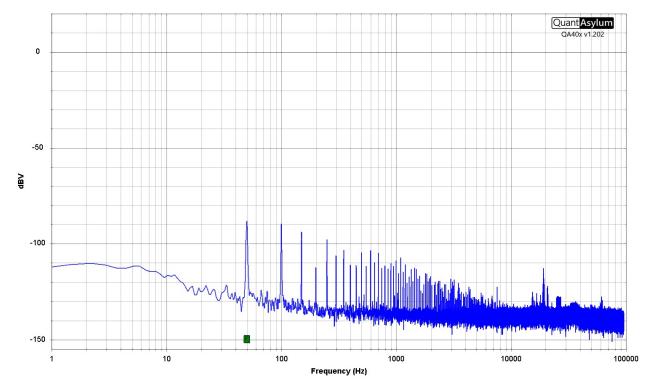


Figure 17 - The noise floor of amplifier is below -90 dBV.

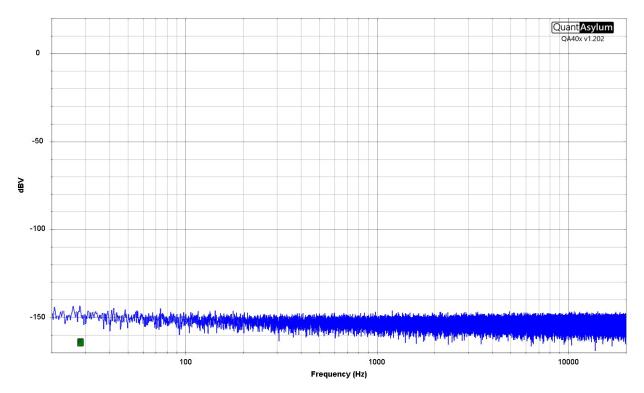


Figure 18 - The noise floor of the measurement device (QA403) is at -150 dBV.

THD simulation vs Measurement

Images of a simulation (upper image) and actual measurements (lower image) of the original ACA amplifier before modifications where made. Although the y-axis are different it is easy to see the simulation matches the real world measurement quite well.

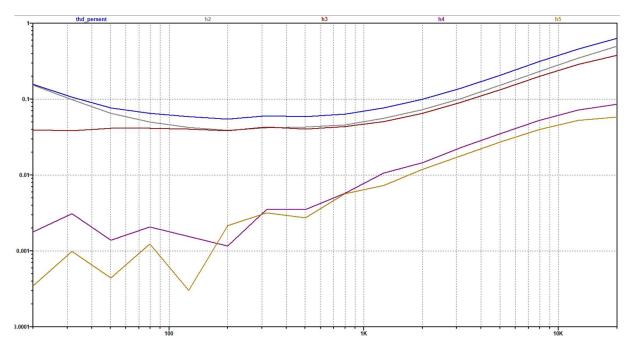


Figure 19 - Simulated THD

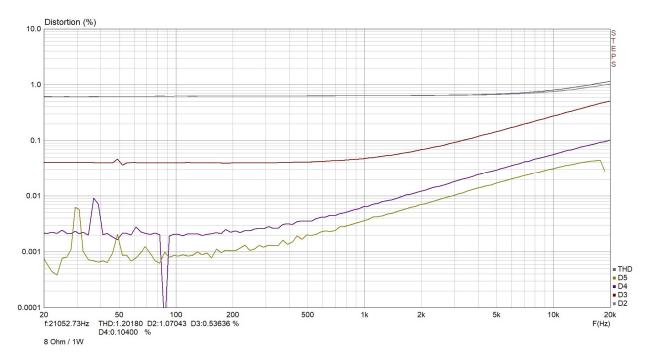


Figure 20 - Measured THD

Gate resistors

A measurement of the original ACA amplifier with and without the original gate-resistors of the power mosfets. Removing the resistors gives a dramatic improvement on the third harmonic (D3). The original gate resistors are too large and slow down the charging of the gate-capacitances, which causes slew rate distortion at higher frequencies. With the resistors the distortion starts to rise at 400 Hz. Without the resistors it starts to rise at 2 kHz.

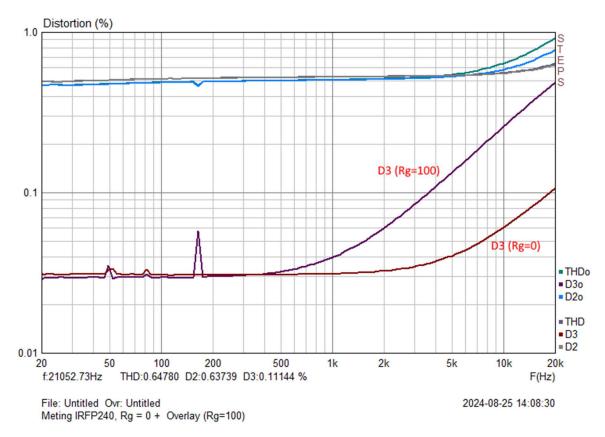


Figure 21 - THD vs frequeny with and without gate-resistors

In the final design 1 Ω gate resistors are used.

Replacing the jfet

Below a simulation where the LSK170B jfet has been replaced by a depletion-mode mosfet DN2540. The current has been increased from 4.5mA to 15mA. The measurements has been done without negative feedback. It is clearly to see that the distortion has become less at higher frequencies.

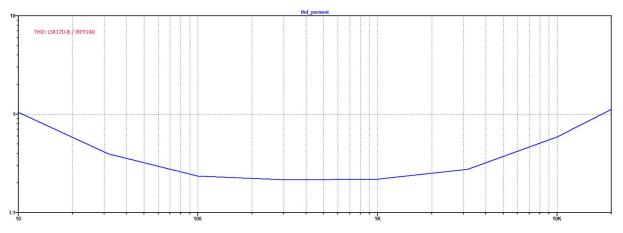


Figure 22 - Distortion with the LSK170B jfet

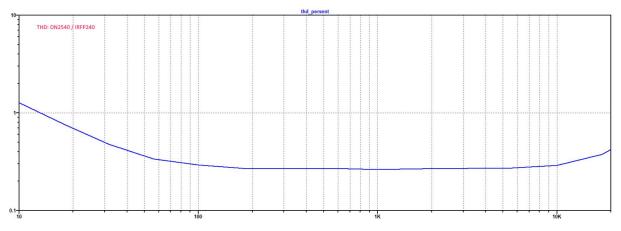


Figure 23 - Distortion with the DN2540 mosfet

Distortion measurements

The distortion of the amplifier measured as a function of frequency.

The distortion is about 0.02 % between 100 Hz and 5 kHz. The distortion is about 10x lower than the design without our modifications.

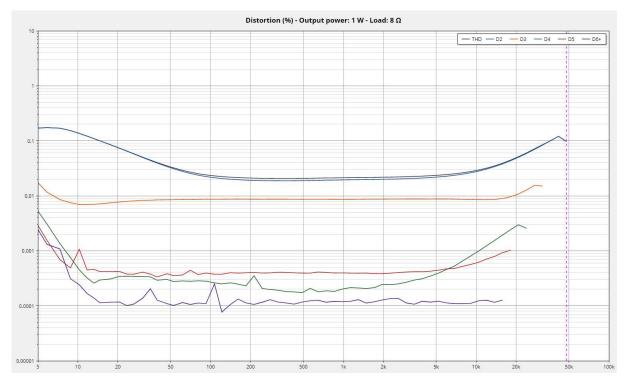


Figure 24 - Distortion vs frequency. THD around 0.02%

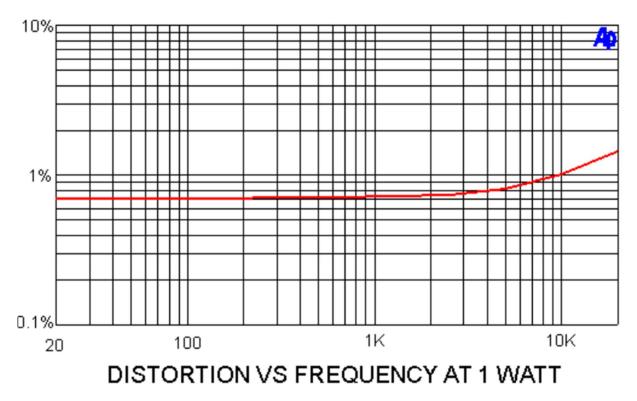
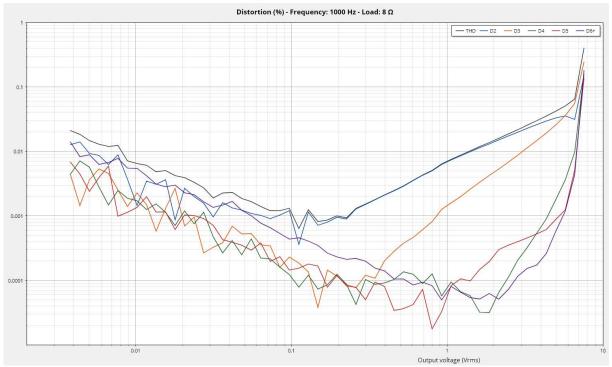
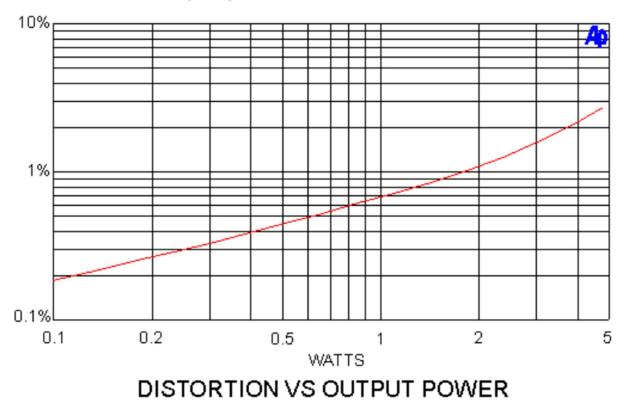


Figure 25 - The original ACA distortion figure. THD around 0.7%



The distortion as a function of output amplitude is shown below.

Figure 26 - Distortion vs output amplitude



Distortion vs output power

Figure 27 - The original ACA distortion vs output power from 0.2% at 0.1W to 2.8% at 5W

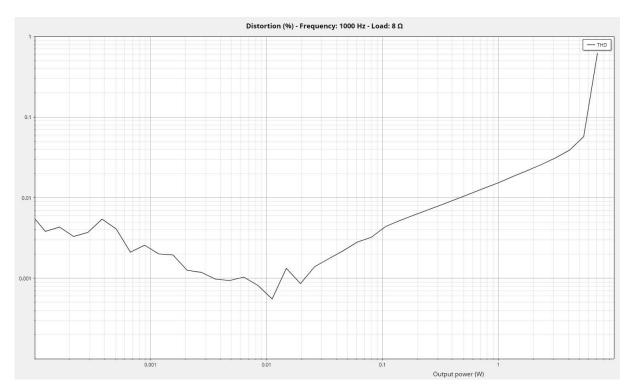


Figure 28 - Distortion vs output power of our amplifier from 0.044% at 0.1W to 0.05% at 5W

Bandwidth

The amplifier's bandwidth is 226 kHz in simulation, but in practice, it measures around 150 kHz. This difference arises because many of the components used in the simulation are idealized, which doesn't reflect real-world conditions.

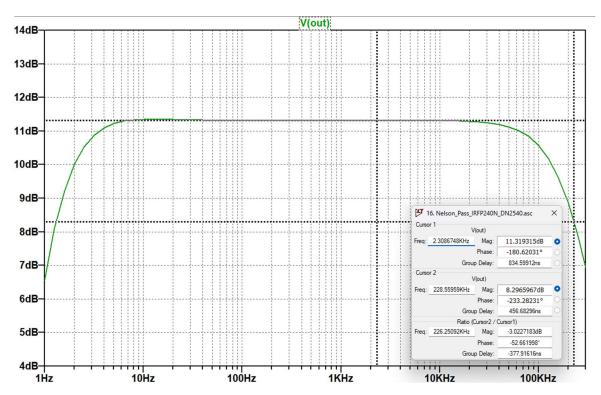


Figure 29 - Simulated bandwidth

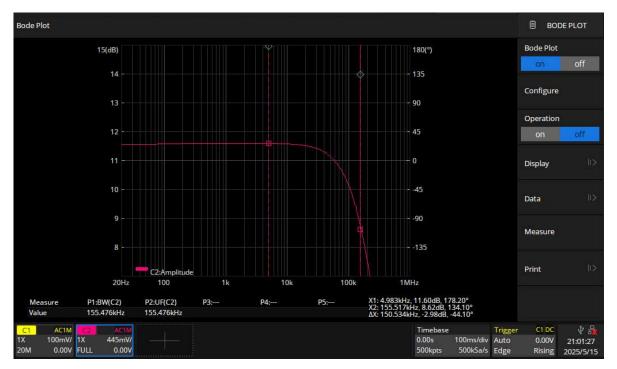


Figure 30 - Bandwidth measured with the oscilloscope and function generator.

Output impedance

The output impedance of the amplifier was simulated to be 0.4 Ω . The measurement shows it was actually 0.4 Ω . The damping factor with a 8 Ω load is therefore 20.

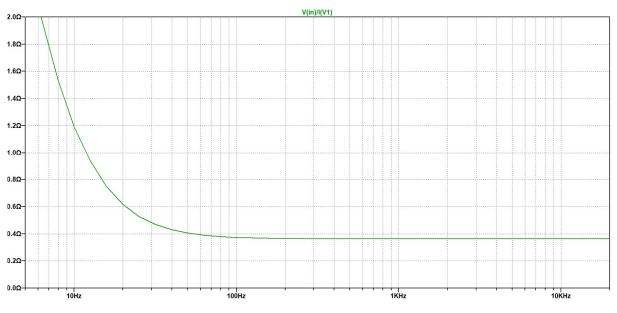


Figure 31 - Simulated output impedance

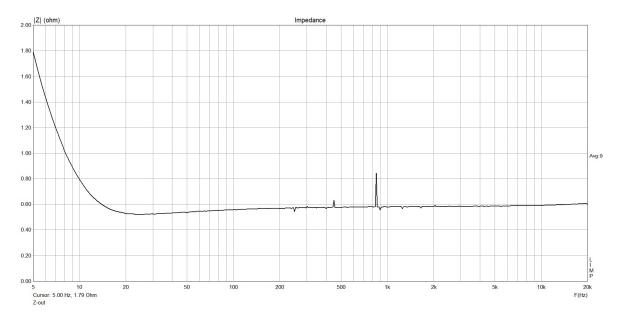
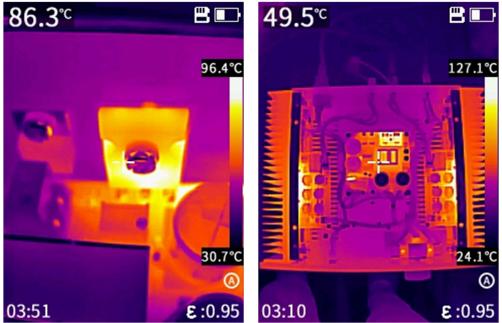


Figure 32 - Measured output impedance

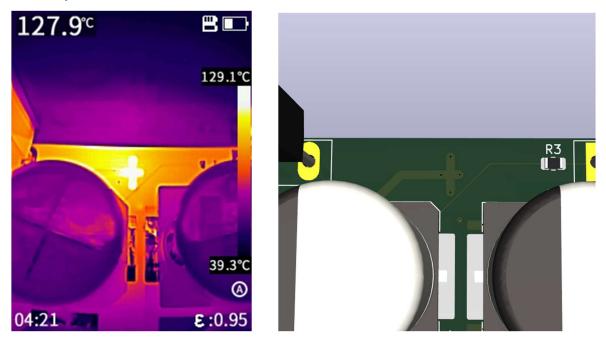
Heat dissipation

Below some infra-red photos of the mosfet and the inside of the chassis.



The mosfets heat up to about 97 °C. At the right a thermal image of the amplifier.

Hotspot



Unfortunately, there is a hotspot on the amplifier pcb where a top-side trace connects to the bottom side through four vias. The current of about 1.9 A causes the vias to heat up to around 130 °C. In future designs, a larger area with more vias should be implemented to reduce this issue. As a quick fix, drilling a hole and connecting both layers with a wire can help. However, since the PCB has two inner layers carrying the power supply voltage and ground, an insulator must be used to prevent shorting the wire to those layers.

Heatsink calculations

Calculations where made to determine the size of the heatsink.

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$$\frac{P_{undias} = 21.0 W}{P_{undias} = 60 W}$$

$$\frac{P_{tit} = P_{2.0}W}{P_{tit} = P_{2.0}W}$$

$$\frac{1}{23.0 W} \quad \frac{1}{100} = 1000 C$$

$$\frac{1}{23.0 W} \quad \frac{1}{100} = 0.000 C$$

$$\frac{1}{23.0 W} \quad \frac{1}{100} = 0.000 C$$

$$\frac{1}{100} \quad \frac{1}{100} = 0.000 C$$

The power supply dissipates 22.8 W and the amplifier dissipates 60 W, totaling 82.8 W. Calculations indicate that a heatsink with a thermal resistance of at most 0.22 °C/W is required. The amplifier chassis purchased includes two heatsinks rated at 0.67 °C/W each, which combined provide 0.34 °C/W. As a result, the heatsinks are expected to reach slightly above 44°C (19°C + 25°C). In reality, however, they heat up to around 53°C.

